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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 400
TROY, MI 48098

EXAMINER	
TSAI, SHENG JEN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/679,030	**Applicant(s)** ARMSTRONG ET AL.	
	Examiner Sheng-Jen Tsai	**Art Unit** 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 September 2006.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-195 is/are pending in the application.
4a) Of the above claim(s) 2,16,28,46,57,61,75,87,105,116,128,138,152 and 161 is/are withdrawn from consideration.
5)☒ Claim(s) 14,15,55,56,73,74,114,115,126,127,159,160,175,176,191 and 192 is/are allowed.
6)☒ Claim(s) 1,3-13,17-27,29-45,47-54,58-60,62-72,76-86, 88-104, 106-113,117-125,129-137, 139-151,153-158,162-174, 177-190 and 193-195 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Request for Continued Examination (RCE) filed on 9/16/2006 regarding application 10,679,030 filed on 10/3/2003.

2. Claims 1, 18, 30, 37, 43, 60, 77, 89, 96, 102, 119, 130, 140, 146, 151, 164 and 180 have been amended.

Claims 2, 16, 28, 46, 57, 61, 75, 87, 105, 116, 128, 138, 152 and 161 have been cancelled.

Claims 1, 3-15, 17-27, 29-45, 47-56, 58-60, 62-74, 76-86, 88-104, 106-115, 117-127, 129-137, 139-151, 153-160 and 162-195 are pending for consideration.

3. *Response to Amendments and Remarks*

Applicant's amendments and remarks have been fully and carefully considered. In response, a new ground of claim analysis based on a newly identified reference (Subrahamanyan et al., US Patent Application Publication 2003/0002198) has been made. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 146-147, 149-151, 153, 155-157, 164-165, 167-168, 170-171, 180-181, 183-184 and 186-187 are rejected under 35 U.S.C. 102(e) as being anticipated by Subrahamanyan et al. (US Patent Application Publication 2003/0002198).

As to claim 146, Subrahamanyan et al. disclose **a method** [High Bandwidth Large Stroke Spin-Stand for Data Storage Component Testing (title)] **for operating a data storage device control circuit** [the corresponding control circuit is the spin-stand (figure 2, 202) including the spindle/XY controller (figure 2, 210), the VCM (figure 2, 234), the R/W control board (figure 2, 228) and the encoder DSP board (figure 2, 240)] **for a data storage device** [the data storage disk, figure 2, 206; figure 1, 110] **that interfaces with an application circuit** [the corresponding application circuit comprising the C67 DSP board (figure 2, 218), the R/W interface board (figure 2, 226), the breakout board (figure 2, 224), the GPIB board (figure 2, 212) and the serial board (figure 2, 216)] **implemented on an application printed circuit board (PCB)** [the corresponding application printed circuit board is the control subsystem (figure 2, 204) comprising the C67 DSP board (figure 2, 218), the breakout board (figure 2, 224), the R/W interface module (figure 2, 226), the serial board (figure 2, 216) and the GPIB board (figure 2, 212)], **comprising**:

receiving data to be stored on the data storage device from the application circuit at said data storage device control circuit [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as

ASCII strings from the COM port 214 (paragraph 0024); Data (including servo data) is magnetically stored on concentric tracks patterned on the disc (paragraph 0003)]; **and receiving data storage device control data including at least one of arm position data and spindle control data from the application circuit at said data storage device control circuit** [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037].

As to claim 147, Subrahamanyan et al. teach that **the method of claim 146 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB)** [figures 1 and 2].

As to claim 149, Subrahamanyan et al. teach that **the method of claim 146 further comprising using a parallel interface for communications between said data storage device control circuit and said application circuit** [The encoder position is available as a 28-bit word generated from the interpolation by the encoder DSP board 240, which is coupled to the breakout board 224 via a 64-conductor ribbon cable (paragraph 0028)].

As to claim 150, Subrahamanyan et al. teach that **the method of claim 146 further comprising implementing said data storage device control circuit using an integrated circuit** [figure 2, 228, 242 and 240].

As to claim 151, Subrahamanyan et al. **disclose a method for providing an architecture for a data storage device** [figures 1 and 2], **comprising**:

storing application data and data storage device control data [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); Data (including servo data) is magnetically stored on concentric tracks patterned on the disc (paragraph 0003); As discussed above, the timer set sampling mode is independent of servo data read from a data storage disc, making it useful for writing servo data to an unwritten data storage disc (paragraph 0040)] **in an application circuit implemented on an application printed circuit board (PCB)** [the corresponding application printed circuit board is the control subsystem (figure 2, 204) comprising the C67 DSP board (figure 2, 218), the breakout board (figure 2, 224), the R/W interface module (figure 2, 226), the serial board (figure 2, 216) and the GPIB board (figure 2, 212)];

mapping logical addresses to physical addresses using said application circuit [a track ID and other disc characteristics may be input to the control subsystem, which would generate an appropriate radial or angular position corresponding to the desired track (paragraph 0044)];

transmitting data to be stored on the data storage device from said application circuit to a data storage device control circuit implemented on a data storage device assembly (DSDA) PCB [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); Data (including servo data) is magnetically stored on concentric tracks patterned on the disc (paragraph 0003); As discussed above, the timer set sampling mode is independent of servo data read from a data storage disc, making it useful for writing servo data to an unwritten data storage disc (paragraph 0040)]; and

transmitting data storage device control signals including at least one of read/write arm position data and spindle control data from said application circuit to said data storage device control circuit [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037].

As to claim 153, Subrahamanyan et al. teach that **the method of claim 151 further comprising at least one of mapping logical addresses to physical addresses** [a track ID and other disc characteristics may be input to the control subsystem, which would generate an appropriate radial or angular position corresponding to the desired track (paragraph 0044)] **and monitoring a location of a read/write head of a data storage device** [paragraph 0027].

As to claim 155, Subrahamanyan et al. teach that **the method of claim 151 further comprising using a parallel interface for communications between said data storage device control circuit and said application circuit** [The encoder position is available as a 28-bit word generated from the interpolation by the encoder DSP board 240, which is coupled to the breakout board 224 via a 64-conductor ribbon cable (paragraph 0028)].

As to claim 156, Subrahamanyan et al. teach that **the method of claim 151 further comprising implementing said application circuit using a first integrated circuit** [figure 2, 220, 218 and 226].

As to claim 157, Subrahamanyan et al. teach that **the method of claim 151 further comprising implementing said data storage device control circuit using a second integrated circuit** [figure 2, 228, 242 and 240].

As to claim 164, Subrahamanyan et al. disclose **a processor chipset** [figure 2, 204] **that communicates with a data storage device** [the data storage disk, figure 2, 206], **comprising**:

an input/output (I/O) circuit that provides an I/O interface for at least one of serial, audio, basic input/output system (BIOS), local area network, mouse, and keyboard connections [figure 2 shows the I/O circuit including serial port (214), serial board (216), breakout board (224) and read/write interface (226)] **and that includes**:

a mapping driver that maps logical addresses to physical addresses [a track ID and other disc characteristics may be input to the control subsystem, which would generate an appropriate radial or angular position corresponding to the desired track (paragraph 0044)];

a data storage device controller (DSDC) [spindle/XY controller (figure 2, 210) and encoder DSP board (figure 2, 240)] **that communicates with said mapping driver and that controls the data storage device** [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037]; **and**

a first I/O interface [the serial port, figure 2, 214] **that communicates with at least one of said DSDC and said mapping driver, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said first I/O interface to the data storage device and said processor chipset is implemented on an application printed circuit board PCB** [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037].

As to claim 165, Subrahamanyan et al. teach that **the processor chipset of Claim 164 further comprising a processor** [the C67 DSP is the corresponding processor] **that performs at least one of data and control processing and that communicates with said I/O circuit** [figure 2; The control subsystem 204 provides fast rotary axis control of the VCM 234 using a 'C67 DSP board 218 plugged into a standard PCI slot in a host computer (paragraph 0032)].

As to claim 167, Subrahamanyan et al. teach that **the processor chipset of Claim 164 wherein said processor chipset communicates with a data storage device control circuit that includes a second I/O interface and at least one of a spindle motor driver, a read/write arm driver, and a read channel driver, and wherein said first I/O interface communicates with said second I/O interface** [figure 2].

As to claim 168, Subrahamanyan et al. teach that **the processor chipset of Claim 167 wherein at least one of said DSDC and said mapping driver communicates data and control information to said read channel in-band over a serial link** [The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037].

As to claim 170, Subrahamanyan et al. teach that **the processor chipset of Claim 167 wherein the data storage device includes:**

a data storage device platter [figure 2, 206]; **a read/write arm** [figure 4; figure 2, 232];

a read/write head arranged on said read/write arm [figure 4; figure 2, 232];;

a spindle motor [figure 2, 207] **that communicates with said spindle motor driver** [figure 2, 210] **and that rotates said data storage device platter** [figure 2, 208];

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm [paragraph 0036-0037]; **and**

a preamp circuit [figure 2, 230] **that communicates with said read channel driver** [figure 2, 228] **and said read/write head** figure 2, 232].

As to claim 171, Subrahamanyan et al. teach that **the processor chipset of Claim 164 wherein said mapping driver at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of the data storage device** [a track ID and other disc characteristics may be input to the control subsystem, which would generate an appropriate radial or angular position corresponding to the desired track (paragraph 0044)].

As to claim 180, refer to "As to claim 164."

As to claim 181, refer to "As to claim 164."

As to claim 183, refer to "As to claim 167."

As to claim 184, refer to "As to claim 168."

As to claim 186, refer to "As to claim 170."

As to claim 187, refer to "As to claim 171."

6. The following claims are rejected under 35 U.S.C. 102(e) as being anticipated by Subrahamanyan et al. (US Patent Application Publication 2003/0002198), by the same reasons as explained in the previous section.

As to claim 1, refer to “As to claim 146” and “As to claim 164.”

As to claim 3, refer to “As to claim 170.”

As to claim 4, refer to “As to claim 150.”

As to claim 5, refer to “As to claim 170.”

As to claim 6, refer to “As to claim 153.”

As to claim 8, refer to “As to claim 155.”

As to claim 9, refer to “As to claim 156.”

As to claim 12, refer to “As to claim 157.”

As to claim 18, refer to “As to claim 164.”

As to claim 19, refer to “As to claim 146.”

As to claim 20, refer to “As to claim 146.”

As to claim 21, refer to “As to claim 146.”

As to claim 22, refer to “As to claim 164.”

As to claim 24, refer to “As to claim 155.”

As to claim 25, refer to “As to claim 156.”

As to claim 30, refer to “As to claim 164.”

As to claim 31, refer to “As to claim 164.”

As to claim 32, refer to “As to claim 164.”

As to claim 34, refer to “As to claim 155.”

As to claim 36, refer to “As to claim 156.”

As to claim 37, refer to “As to claim 164.”

As to claim 38, refer to “As to claim 164.”

As to claim 39, refer to "As to claim 164."

As to claim 41, refer to "As to claim 155."

As to claim 42, refer to "As to claim 156."

As to claim 43, refer to "As to claim 164."

As to claim 44, refer to "As to claim 170."

As to claim 45, refer to "As to claim 156."

As to claim 47, refer to "As to claim 170."

As to claim 48, refer to "As to claim 164."

As to claim 50, refer to "As to claim 155."

As to claim 51, refer to "As to claim 156."

As to claim 53, refer to "As to claim 157."

As to claim 59, refer to "As to claim 156."

As to claim 60, refer to "As to claim 164."

As to claim 62, refer to "As to claim 164" and "As to claim 170."

As to claim 63, refer to "As to claim 146."

As to claim 64, refer to "As to claim 170."

As to claim 65, refer to "As to claim 153."

As to claim 67, refer to "As to claim 149."

As to claim 68, refer to "As to claim 156."

As to claim 71, refer to "As to claim 157."

As to claim 77, refer to "As to claim 164."

As to claim 78, refer to "As to claim 146."

As to claim 79, refer to "As to claim 146."

As to claim 80, refer to "As to claim 146."

As to claim 83, refer to "As to claim 155."

As to claim 84, refer to "As to claim 156."

As to claim 89, refer to "As to claim 164" and "As to claim 170."

As to claim 90, refer to "As to claim 146."

As to claim 91, refer to "As to claim 146."

As to claim 93, refer to "As to claim 155."

As to claim 95, refer to "As to claim 156."

As to claim 96, refer to "As to claim 164."

As to claim 97, refer to "As to claim 146."

As to claim 98, refer to "As to claim 146."

As to claim 100, refer to "As to claim 155."

As to claim 101, refer to "As to claim 156."

As to claim 102, refer to "As to claim 164" and "As to claim 170."

As to claim 103, refer to "As to claim 170."

As to claim 104, refer to "As to claim 146."

As to claim 106, refer to "As to claim 170."

As to claim 107, refer to "As to claim 153."

As to claim 109, refer to "As to claim 155."

As to claim 110, refer to "As to claim 156."

As to claim 112, refer to "As to claim 157."

As to claim 118, refer to “As to claim 156.”

As to claim 119, refer to “As to claim 164.”

As to claim 120, refer to “As to claim 146.”

As to claim 121, refer to “As to claim 153.”

As to claim 123, refer to “As to claim 155.”

As to claim 130, refer to “As to claim 164.”

As to claim 131, refer to “As to claim 146.”

As to claim 132, refer to “As to claim 146.”

As to claim 133, refer to “As to claim 164.”

As to claim 135, refer to “As to claim 155.”

As to claim 136, refer to “As to claim 156.”

As to claim 140, refer to “As to claim 164.”

As to claim 141, refer to “As to claim 146.”

As to claim 143, refer to “As to claim 155.”

As to claim 145, refer to “As to claim 156.”

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3-8, 11-16, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US Patent Application Publication 2005/0005044), and in view of Subrahamanyan et al. (US Patent Application Publication 2003/0002198).

As to claim 1, Liu et al. disclose **an architecture for a data storage device** [Storage Virtualization Computer System and External Controller Therefor (title)] , **comprising**:

A data storage device assembly (DSDA) printed circuit board (PCB) [Liu et al.: it is also significantly more expensive and occupies a significantly larger footprint on a printed circuit board (PCB) per interconnect than either P-ATA or S-ATA; fiber interconnects do not scale well because of the size of the footprint on the PCB and cost per interconnect, typically being an order of magnitude greater than P-ATA/S-ATA (paragraph 0090); also see Subrahamanyan et al.: figure 2] **including a first data storage device control circuit** [the PCI-X to SATA controller (figure 7, 310; figure 8) which is part of the SATA I/O device interconnect controller (figure 4, 300)] **that includes a first input/output (I/O) interface** [figures 7 and 8 show the first I/O interface connecting to an array of external Physical Storage devices (PSD)]; **and**

An application PCB [Liu et al.: it is also significantly more expensive and occupies a significantly larger footprint on a printed circuit board (PCB) per interconnect than either P-ATA or S-ATA; fiber interconnects do not scale well because of the size of the footprint on the PCB and cost per interconnect, typically being an order of magnitude greater than P-ATA/S-ATA (paragraph 0090); also see Subrahamanyan et al.: figure 2] **including an application circuit** [the Storage Virtualization Controller (SVC) shown in figures 3 and 4] **including a buffer** [the corresponding buffer comprises a memory unit (figure 4, 280) and a NVRAM unit (figure 5, 248)] **that stores application data** [the memory 280 is connected to the CPC 240 and acts as a buffer to buffer the data transferred between the host entity 10 and the PSD array 400 through the CPC 240 (paragraph 0054)] **and data storage device control data** [the NVRAM is provided for saving some information regarding the IO operation execution status of the array which can be examined after an abnormal power shut-off occurs in the event that IO operation execution does not complete (paragraph 0057)], **a mapping driver that maps logical addresses to physical addresses** [a Storage virtualization Controller, abbreviated SVC, is a device the primary purpose of which is to map combinations of sections of physical storage media to logical media units visible to a host system. IO requests received from the host system are parsed and interpreted and associated operations and data are translated into physical storage device IO requests. This process may be indirect with operations cached, delayed (e.g., write-back), anticipated (read-ahead), grouped, etc. to improve performance and other operational characteristics so that a host IO request may not necessarily result directly in physical storage device IO requests in a one-to-one fashion (paragraph 0005); the primary function of a storage virtualization controller, abbreviated as SVC, is to manage, combine, and manipulate physical storage devices in such a way as to present them as a set of logical media units to the host. Each LMU is presented to the host as if it were a directly-connected physical storage device (PSD) of which the LMU is supposed to be the logical equivalent. In order to accomplish this, IO requests sent out by the host to be processed by the SVC that will normally generate certain behavior in an equivalent PSD also generate logically equivalent behavior on the part of the SVC in relation to the addressed logical media unit. The result is that the host "thinks" it is directly connected to and communicating with a PSD when in actuality the host is connected to a SVC that is simply emulating the behavior of the PSD of which the addressed logical media unit is the logical equivalent (paragraph 0010)], **and a second I/O interface** [the PCI interface to SATA I/O device interconnect controller (figure 6, 932)] **that communicates with at least one of said buffer and said mapping driver** [figures 4-9; paragraphs 0058-0060], **wherein said control data includes at least one of arm position and spindle control data** [by Subrahamanyan et al., see below] **and said physical addresses and data are transmitted by said second I/O interface to said first I/O interface** [figures 4-9; paragraph 0055]; .

Regarding claim 1, Liu et al. do not mention that the control data includes at least one of arm position and spindle control data.

However, Subrahamanyan et al. disclose in their invention “High Bandwidth Large Stroke Spin-Stand for Data Storage Component Testing” an apparatus and method of testing a DSDA [figures 1 and 2] where a host computer commands a control subsystem [figure 2, 204] to send desired read/write arm positions as well as spindle data to a spin-stand [figure 2, 202] to control the storage data disk [figure 2, 206; The rotation (e.g., rotation speed) of the spindle 208 by the spindle motor 207 and the XY position of the head are controlled by the control subsystem 204 through the COM port 214 and a spindle/XY controller 210. Spindle rotation and stage positioning parameters are transmitted as ASCII strings from the COM port 214 (paragraph 0024); paragraphs 0036-0037].

While Liu et al. do not mention the details of low-level operations associated with a storage data device, Subrahamanyan et al. address this particular aspect and the need for a high bandwidth, large stroke spin-stand for testing components of data storage devices [paragraph 0003-0007].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the need of being able to control arm positions and spindle operations of a storage device, as demonstrated by Subrahamanyan et al., and to incorporate this feature into the existing scheme disclosed by Liu et al. to further improve the reliability of the storage devices.

As to claim 3, Liu et al. teach that **the storage devices the data storage device architecture of claim 1 wherein said first data storage device control circuit includes a data storage device controller (DSDC)** [the SVC, figures 3-9], **a data storage device processor** [the central processing circuit unit (figure 4, 240; figure 5)], **a spindle motor driver** [see Subrahamanyan et al., figure 2, 207 and 210], **a read/write arm driver** [see Subrahamanyan et al., figure 2, 232 and figure 4], **and a read channel driver** [see Subrahamanyan et al., figure 2, 228], **wherein said DSDC communicates with said first I/O interface** [figures 7 and 8 show the first I/O interface connecting to an array of external Physical Storage devices (PSD)] **and with at least one of said data storage device processor** [the CPU (figure 5, 242); figure

6], **said spindle motor driver, said read/write arm driver, and said read channel driver** [see Subrahamanyan et al., figure 2].

As to claim 4, Subrahamanyan et al. teach **the use of an application specific integrated circuit** [the PEM-FPGA, figure 2, 220] **and an application processor** [the C67 DSP, figure 2, 218].

As to claim 5, Subrahamanyan et al. teach that **the processor chipset of Claim 3 wherein the data storage device includes**:

a data storage device platter [figure 2, 206]; **a read/write arm** [figure 4; figure 2, 232];

a read/write head arranged on said read/write arm [figure 4; figure 2, 232];;

a spindle motor [figure 2, 207] **that communicates with said spindle motor driver** [figure 2, 210] **and that rotates said data storage device platter** [figure 2, 208];

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm [paragraph 0036-0037]; **and**

a preamp circuit [figure 2, 230] **that communicates with said read channel driver** [figure 2, 228] **and said read/write head** figure 2, 232].

As to claim 6, Liu et al. teach that **the mapping driver at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of a data storage device** [a Storage virtualization Controller, abbreviated SVC, is a device the primary purpose of which is to map combinations of sections of physical storage media to logical media units visible to a host system. IO requests received from the host system are parsed and interpreted and associated operations and data are translated into physical storage device IO requests. This process may be indirect with operations cached, delayed (e.g., write-back), anticipated (read-ahead), grouped, etc. to improve performance and other operational characteristics so that a host IO request may not necessarily result directly in physical storage device IO requests in a one-to-one fashion (paragraph 0005); the primary function of a storage virtualization controller, abbreviated as SVC, is to manage, combine, and manipulate physical storage devices in such a way as to present them as a set of logical media units to the host. Each LMU is presented to the host as if it were a directly-connected physical storage device (PSD) of which the LMU is supposed to be the logical equivalent. In order to accomplish this, IO requests sent out by the host to be processed by the SVC that will normally generate certain behavior in an equivalent PSD also generate logically equivalent behavior on the part of the SVC in relation to the addressed logical media unit. The result is that the host "thinks" it is directly connected to and communicating with a PSD when in actuality the host is connected to a SVC that is simply emulating the behavior of the PSD of which the addressed logical media unit is the logical equivalent (paragraph 0010)].

As to claim 7, Liu et al. teach that **the first and second I/O interfaces are serial ATA interfaces** [figures 3,7, 8 and 10].

As to claim 8, Liu et al. teach that **the first and second I/O interfaces are parallel interfaces** [this case is shown in figure 1].

As to claim 11, Liu et al. teach that **the application circuit includes a pod multiplier** [figure 8 shows the port multiplier used to interface to a plurality of PSDs].

As to claim 16, refer to "As to claim 2."

As to claim 17, Liu et al. teach that **the data storage device architecture of claim 1 further comprising a plurality of second data storage device control circuits** [the DEC/MUX Arbiter (figure 8, 314) and a plurality of SATA ports; figure 9] **each including a third I/O interface** [figure s 8 and 9], **wherein said port multiplier communicates with said third I/O interface of said second data storage device control circuits** [figure s 8 and 9].

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US Patent Application Publication 2005/0005044), in view of Subrahamanyan et al. (US Patent Application Publication 2003/0002198), and further in view of O'Hare et al. (US 6,553,471).

As to claim 10, neither Liu et al. nor Subrahamanyan et al. mention **the inclusion of a first security module and a second security module in the communication paths**.

However, O'Hare et al. teach in their invention "Controlling Access to a Storage Device by Controlling Communication Ports Thereto" a method and apparatus of coupling a security module (figure 3, 64) to a port driver (figure 3, 62) so that all data going into and out of the data storage device via the port is controlled by the security module (column 5, lines 25-35). O'Hare et al. further teach that more than one such security module (hence a second security module) may be included in a single storage device to support multiple data connections through a plurality of ports (figures 1 and 2).

A security data module in the data path ensures that only authorized users may access the contents of the storage device, and protects the data from being modified by unauthorized users.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the benefits of including a security module in the data/communication paths, as demonstrated by O'Hare et al., and to incorporate it into the existing apparatus disclosed by Liu et al. to further improve the security of the data storage device.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US Patent Application Publication 2005/0005044), in view of Subrahamanyan et al. (US Patent Application Publication 2003/0002198), and further in view of Morris (US 6,418,474).

As to claim 13, neither Liu et al. nor Subrahamanyan et al. mention that **the data request includes an expiration time and that the mapping driver cancels the data request if the DSDC does not respond to the data request before the expiration time**.

However, Morris teaches in the invention "Data Transfer Protocol Flow Controller and Method" a method and protocol of controlling data transfer in which a time-out interval (i.e., the expiration time) is specified and the transaction is terminated if the reply is not received before the time-out (figure 2; abstract).

The use of a time-out interval in a request-and-reply application prevents a faulty device from occupying valuable system resources, hence improving the reliability and availability of the system.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the benefits of imposing an expiration time on the response to a request, as demonstrated by Morris, and to incorporate it into the existing apparatus disclosed by Liu et al. to further improve the reliability and availability of the system.

11. Claim 166 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US Patent Application Publication 2005/0005044), in view of Subrahamanyan et al. (US Patent Application Publication 2003/0002198), and further in view of Wu (US Patent Application Publication 2002/0178320).

As to claim 166, Liu et al. teach the use of **a system bus that transfers data and that communicates with the processor** [figure 5 shows the X-Bus and figure 6 shows the PM Bus];

A peripheral component interconnect (PCI) bus [figure 6, 930 and 932 show the PCI interface] **that communicates with the processor and that provides an interface to an expansion card slot** [figures 17 and 18 show the expansion slots].

With respect to claim 166, neither Liu et al. nor Subrahamanyan et al. mention that **a nothbridge chipset that communicates with the processor over the system bus, and that a southbridge chipset that communicates with the PCI bus**.

However, Wu teaches in the invention "Method and Architecture for Accessing Hardware Devices in Computer System and the Chipset Thereof" a method and architecture of connecting and accessing I/O devices with the use of a northebridge and a southbridge chipsets with a system management bus (SMB) and a PCI bus (abstract; figures 1-5).

The use of northebridge and southbridge chipsets associated with a system bus and a PCI bus allows a large number of peripheral devices to communicate with each other without causing traffic congestion that in turn impacts processor efficiency.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the benefits of using northebridge and southbridge chipsets associated with a system bus and a PCI bus, as demonstrated by Wu, and to incorporate it into the existing apparatus disclosed by Liu et al. to further enhance the performance of the system.

As to claim 168, refer to "As to claim 7."

As to claim 167, refer to "As to claim 3."

As to claim 169, Liu et al. teach that **at least one of said DSDC and said mapping driver communicates data to said read channel in-band** [the memory 280 is connected to the CPC 240 and acts as a buffer to buffer the data transferred between the host entity 10 and the PSD array 400 through the CPC 240 (figure 4; figure 6; paragraph 0054), this data path uses the PCI bus and serves as the in-band route] **and control information to said read channel out-of-band** [the NVRAM is provided for saving some information regarding the IO operation execution status of the array which can be examined after an abnormal power shut-off occurs in the event that IO operation execution does not complete (figure 5; paragraph 0057), this data path uses the X-Bus (figure 5) and serves as the out-of-band route].

12. The following claims are each ejected by the same reasons as the related claim(s) indicated. Refer to the explanation set forth in earlier sections.

As to claim 18, refer to "As to claim 1" and "As to claim 4."

As to claim 19, refer to "As to claim 3."

As to claim 20, refer to "As to claim 1."

As to claim 21, refer to "As to claim 6."

As to claim 22, refer to "As to claim 4."

As to claim 23, refer to "As to claim 7."

As to claim 24, refer to "As to claim 8."

As to claim 25, refer to "As to claim 9."

As to claim 26, refer to "As to claim 11."

As to claim 27, refer to "As to claim 10."

As to claim 28, refer to "As to claim 2."

As to claim 29, refer to "As to claim 17."

As to claim 30, refer to "As to claim 1" and "As to claim 3."

As to claim 31, refer to "As to claim 2."

As to claim 32, refer to "As to claim 1."

As to claim 33, refer to "As to claim 7."

As to claim 34, refer to "As to claim 8."

As to claim 35, refer to “As to claim 10.”

As to claim 36, refer to “As to claim 9.”

As to claim 37, refer to “As to claim 1” and “As to claim 3.”

As to claim 38, refer to “As to claim 2.”

As to claim 39, refer to “As to claim 1.”

As to claim 40, refer to “As to claim 7.”

As to claim 41, refer to “As to claim 8.”

As to claim 42, refer to “As to claim 2.”

As to claim 43, refer to “As to claim 1.”

As to claim 44, refer to “As to claim 3.”

As to claim 45, refer to “As to claim 4.”

As to claim 46, refer to “As to claim 2.”

As to claim 47, refer to “As to claim 5.”

As to claim 48, refer to “As to claim 6.”

As to claim 49, refer to “As to claim 7.”

As to claim 50, refer to “As to claim 8.”

As to claim 51, refer to “As to claim 9.”

As to claim 52, refer to “As to claim 11.”

As to claim 53, refer to “As to claim 12.”

As to claim 54, refer to “As to claim 13.”

As to claim 57, refer to “As to claim 2.”

As to claim 58, refer to “As to claim 17.”

As to claim 59, refer to “As to claim 12.”

As to claim 60, refer to “As to claim 1.”

As to claim 61, refer to “As to claim 2.”

As to claim 62, refer to “As to claim 3.”

As to claim 63, refer to “As to claim 1.”

As to claim 64, refer to “As to claim 5.”

As to claim 65, refer to “As to claim 6.”

As to claim 66, refer to “As to claim 7.”

As to claim 67, refer to “As to claim 8.”

As to claim 68, refer to “As to claim 9.”

As to claim 69, refer to “As to claim 10.”

As to claim 70, refer to “As to claim 11.”

As to claim 71, refer to “As to claim 12.”

As to claim 72, refer to “As to claim 13.”

As to claim 75, refer to “As to claim 2.”

As to claim 76, refer to “As to claim 17.”

As to claim 77, refer to “As to claim 1.”

As to claim 78, refer to “As to claim 1” and “As to claim 3.”

As to claim 79, refer to “As to claim 1.”

As to claim 80, refer to “As to claim 61.”

As to claim 81, refer to “As to claim 4.”

As to claim 82, refer to “As to claim 7.”

As to claim 83, refer to "As to claim 8."

As to claim 84, refer to "As to claim 9."

As to claim 85, refer to "As to claim 11."

As to claim 86, refer to "As to claim 10."

As to claim 87, refer to "As to claim 12."

As to claim 88, refer to "As to claim 17."

As to claim 89, refer to "As to claim 1" and "As to claim 3."

As to claim 90, refer to "As to claim 2."

As to claim 91, refer to "As to claim 1."

As to claim 92, refer to "As to claim 7."

As to claim 93, refer to "As to claim 8."

As to claim 94, refer to "As to claim 10."

As to claim 95, refer to "As to claim 12."

As to claim 96, refer to "As to claim 1" and "As to claim 3."

As to claim 97, refer to "As to claim 2."

As to claim 98, refer to "As to claim 6."

As to claim 99, refer to "As to claim 7."

As to claim 100, refer to "As to claim 8."

As to claim 101, refer to "As to claim 12."

As to claim 102, refer to "As to claim 1."

As to claim 103, refer to "As to claim 3."

As to claim 104, refer to "As to claim 1."

As to claim 105, refer to “As to claim 2.”

As to claim 106, refer to “As to claim 5.”

As to claim 107, refer to “As to claim 6.”

As to claim 108, refer to “As to claim 7.”

As to claim 109, refer to “As to claim 8.”

As to claim 110, refer to “As to claim 12.”

As to claim 111, refer to “As to claim 11.”

As to claim 112, refer to “As to claim 2.”

As to claim 113, refer to “As to claim 13.”

As to claim 116, refer to “As to claim 2.”

As to claim 117, refer to “As to claim 17.”

As to claim 118, refer to “As to claim 2.”

As to claim 119, refer to “As to claim 1.”

As to claim 120, refer to “As to claim 2.”

As to claim 121, refer to “As to claims 3 and 6.”

As to claim 122, refer to “As to claim 7.”

As to claim 123, refer to “As to claim 8.”

As to claim 124, refer to “As to claim 10.”

As to claim 125, refer to “As to claim 13.”

As to claim 128, refer to “As to claim 2.”

As to claim 129, refer to “As to claim 11.”

As to claim 130, refer to “As to claim 1.”

As to claim 131, refer to “As to claim 3.”

As to claim 132, refer to “As to claim 1.”

As to claim 133, refer to “As to claim 6.”

As to claim 134, refer to “As to claim 7.”

As to claim 135, refer to “As to claim 8.”

As to claim 136, refer to “As to claim 9.”

As to claim 137, refer to “As to claim 10.”

As to claim 138, refer to “As to claim 2.”

As to claim 139, refer to “As to claim 17.”

As to claim 140, refer to “As to claim 1.”

As to claim 141, refer to “As to claim 2.”

As to claim 142, refer to “As to claim 7.”

As to claim 143, refer to “As to claim 8.”

As to claim 144, refer to “As to claim 10.”

As to claim 145, refer to “As to claim 12.”

As to claim 146, refer to “As to claim 1.”

As to claim 147, refer to “As to claim 2.”

As to claim 148, refer to “As to claim 7.”

As to claim 149, refer to “As to claim 8.”

As to claim 150, refer to “As to claim 9.”

As to claim 151, refer to “As to claim 1.”

As to claim 152, refer to “As to claim 2.”

As to claim 153, refer to “As to claims 3 and 6.”

As to claim 154, refer to “As to claim 7.”

As to claim 155, refer to “As to claim 8.”

As to claim 156, refer to “As to claim 9.”

As to claim 157, refer to “As to claim 12.”

As to claim 158, refer to “As to claim 13.”

As to claim 161, refer to “As to claim 2.”

As to claim 162, refer to “As to claim 17.”

As to claim 163, refer to “As to claim 9.”

As to claim 164, refer to “As to claim 1.”

As to claim 165, refer to “As to claim 1.”

As to claim 170, refer to “As to claim 5.”

As to claim 171, refer to “As to claims 3 and 6.”

As to claim 172, refer to “As to claim 7.”

As to claim 173, refer to “As to claim 11.”

As to claim 174, refer to “As to claim 13.”

As to claim 177, refer to “As to claim 17.”

As to claim 178, refer to “As to claim 1.” Further, refer to figures 1-5 of Wu.

As to claim 179, refer to “As to claim 1.” Further, refer to figures 1-5 of Wu.

As to claim 180, refer to “As to claim 1.”

As to claim 181, refer to “As to claim 1.”

As to claim 182, refer to “As to claim 166.”

As to claim 183, refer to "As to claim 3."

As to claim 184, refer to "As to claim 168."

As to claim 185, refer to "As to claim 169."

As to claim 186, refer to "As to claim 5."

As to claim 187, refer to "As to claims 3 and 6."

As to claim 188, refer to "As to claim 7."

As to claim 189, refer to "As to claim 11."

As to claim 190, refer to "As to claim 13."

As to claim 193, refer to "As to claim 17."

As to claim 194, refer to "As to claim 178."

As to claim 195, refer to "As to claim 179."

Allowable Subject Matter

13. Claims 14-15, 55-56, 73-74, 114-115, 126-127, 159-160, 175-176 and 191-192 are allowed.

14. *Related Prior Art of Record*

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Graunke et al., (US 5,991,399), "Method for Securely Distributing a Conditional Use Private key to a Trusted Entity on a Remote System."
- Coulson, (US 6,725,342), "non-Volatile Mass Storage Cache Coherency Apparatus."

- Ingman et al., (US Patent Application Publication 2004/0111634), "Security Permissions for an Integrated Dispatch System"
- Gniewek, (US 5,287,459), "Method and Apparatus for Reducing Response Time in Automated Library Data Retrieval systems."

Conclusion

15. Claims 1,3-13,17-27,29-45,47-54,58-60,62-72,76-86, 88-104, 106-113,117-125,129-137, 139-151,153-158,162-174, 177-190 and 193-195 are rejected as explained above.

Claims 14-15, 55-56, 73-74, 114-115, 126-127, 159-160, 175-176 and 191-192 are allowed.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

October 2, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
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